High Speed USB 2.0 (480Mbps) DPDT Analog Switch

GENERAL DESCRIPTION

The SGM7223 is a high-speed, low-power double-pole/ double-throw (DPDT) analog switch that operates from a single +1.8V to +4.3V power supply.

SGM7223 is designed for the switching of high-speed USB 2.0 signals in handset and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB I/Os.

The SGM7223 has low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps). Each switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. Its bandwidth is wide enough to pass high-speed USB 2.0 differential signals (480 Mb/s) with good signal integrity.

The SGM7223 contains special circuitry on the D+/D- pins which allows the device to withstand a V_{BUS} short to D+ or D- when the USB devices are either powered off or powered on.

SGM7223 is available in Pb-free TQFN-10 (2.1mm× 1.6mm) package. It operates over an ambient temperature range of -40℃ to +85℃.

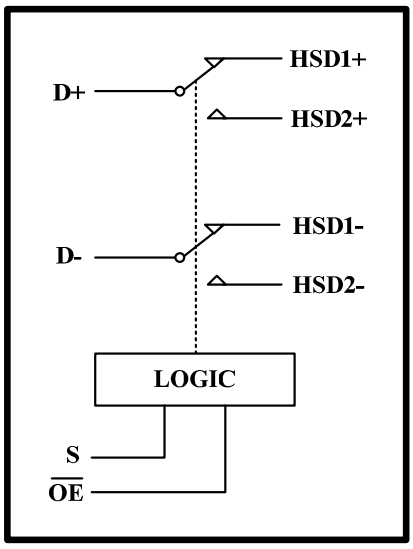
APPLICATIONS

Route Signals for USB 2.0
MP3 and Other Personal Media Players
Digital Cameras and Camcorders
Portable Instrumentation
Set-Top Boxs
PDAs

FEATURES

- **R_{ON} is Typically 4.5Ω at +3.0V**
- **Low Bit-to-Bit Skew: 50ps (TYP)**
- **Voltage Operation : +1.8V to +4.3V**
- **Fast Switching Times:**
  t_{ON} 11ns
  t_{OFF} 20ns
- **Low Crosstalk: -33dB at 250MHz**
- **Power-Off Protection when V_+ = 0V,**
  D+/D- Pins can Tolerate up to 5.25V
- **High Off-Isolation: -30dB at 250MHz**
- **Rail-to-Rail Input and Output Operation**
- **Break-Before-Make Switching**
- **Extended Industrial Temperature Range:**
  -40℃ to +85℃
- **Lead (Pb) Free TQFN-10 (2.1mm × 1.6mm) Package**

BLOCK DIAGRAM



ORDERING INFORMATION

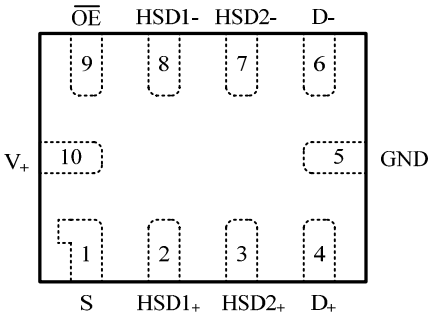
MODEL	PIN-PACKAGE	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKAGE OPTION
SGM7223	TQFN-10 (2.1mm × 1.6mm)	-40℃ to +85℃	SGM7223YTQD10/TR	7223	Tape and Reel, 3000

ABSOLUTE MAXIMUM RATINGS

V_+, IN to GND..... 0V to +4.6V
Analog, Digital voltage range .....-0.3V to (V_++0.3V)
Continuous Current HSDn or Dn…….....±100mA
Peak Current HSDn or Dn…….....±150mA
Operating Temperature Range.....-40℃ to +85℃
Junction Temperature..... +150℃
Storage Temperature.....-65℃ to +150℃
Lead Temperature (soldering, 10s).....+260℃
ESD Susceptibility
HBM.....4000V
MM.....400V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION (TOP VIEW)



PIN DESCRIPTION

TQFN-10 (2.1mm×1.6mm)	NAME	FUNCTION
10	V_+	Power Supply
5	GND	Ground
1	S	Select Input
9	$\overline{OE}$	Output Enable
2, 3, 8, 7, 4, 6	$HSD1_+$, $HSD2_+$, $HSD1_-$, $HSD2_-$, D_+, D_-	Data Ports

FUNCTION TABLE

$\overline{OE}$	S	HSD1+ HSD1-	HSD2+ HSD2-
0	0	ON	OFF
0	1	OFF	ON
1	×	OFF	OFF

Switches Shown For Logic "0" Input

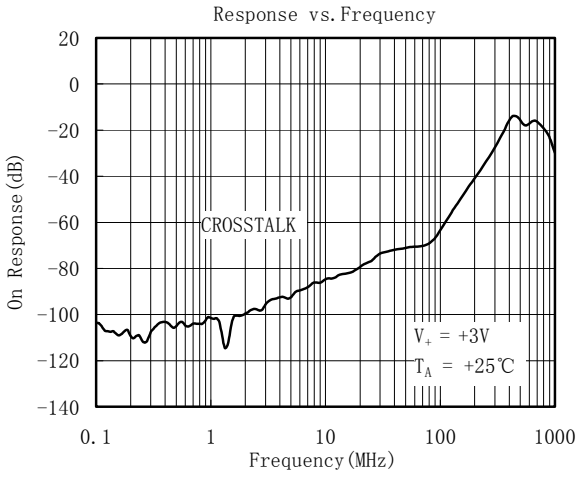
ELECTRICAL CHARACTERISTICS

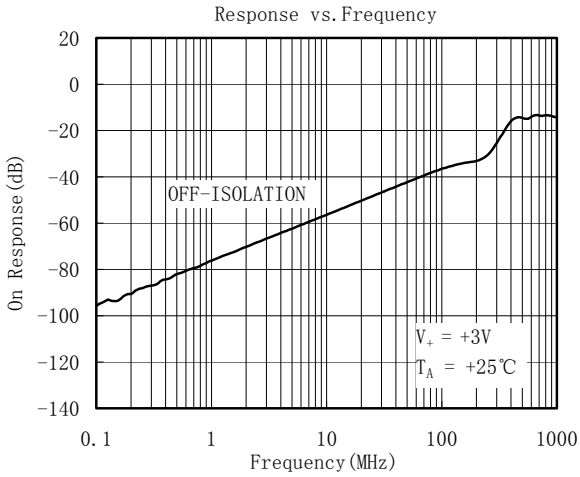
(V_+ = +1.8V to +4.3V, GND = 0V, V_{IH} = +1.6V, V_{IL} = +0.5V, T_A = -40℃ to + 85℃. Typical values are at V_+ = +3.3V, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TPY	MAX	UNITS
ANALOG SWITCH							
Analog I/O Voltage ($HSD1_+$, $HSD1_-$, $HSD2_+$, $HSD2_-$)	V_{IS}		-40℃ to +85℃	0		V_+	V
On-Resistance	R_{ON}	V_+ = 3.0V, V_{IS} = 0V to 0.4V, I_D = 8mA, Test Circuit 1	+25℃		4.5	8.5	Ω
			-40℃ to +85℃			9	
On-Resistance Match Between Channels	ΔR_{ON}	V_+ = 3.0V, V_{IS} = 0V to 0.4V, I_D = 8mA, Test Circuit 1	+25℃		0.2	0.6	Ω
			-40℃ to +85℃			1.5	
On-Resistance Flatness	$R_{FLAT(ON)}$	V_+ = 3.0V, V_{IS} = 0V to 1.0V, I_D = 8mA, Test Circuit 1	+25℃		1.8	2.2	Ω
			-40℃ to +85℃			2.8	
Power Off Leakage Current (D_+, D_-)	I_{OFF}	V_+ = 0V, V_D = 0V to 3.6V, V_S, $V_{\overline{OE}}$ = 0V or 3.6V	-40℃ to +85℃			1	μA
Increase in I_+ per Control Voltage	I_{CCT}	V_+ = 3.6V, V_S or $V_{\overline{OE}}$ = 2.6V	-40℃ to +85℃			5	μA
Source Off Leakage Current	$I_{HSD2(OFF)}$,$I_{HSD1(OFF)}$	V_+ = 3.6V, V_{IS} = 3.3V/ 0.3V, V_D = 0.3V/ 3.3V	-40℃ to +85℃			1	μA
Channel On Leakage Current	$I_{HSD2(ON)}$, $I_{HSD1(ON)}$	V_+ = 3.6V, V_{IS} = 3.3V/ 0.3V, V_D = 3.3V/ 0.3V or floating	-40℃ to +85℃			1	μA
DIGITAL INPUTS							
Input High Voltage	V_{IH}		-40℃ to +85℃	1.6			V
Input Low Voltage	V_{IL}		-40℃ to +85℃			0.5	V
Input Leakage Current	I_{IN}	V_+ = 3.0V, V_S, $V_{\overline{OE}}$ = 0V or V_+	-40℃ to +85℃			1	μA
DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	V_{IS} = 0.8V, R_L = 50Ω, C_L = 10pF, Test Circuit 2	+25℃		11		ns
Turn-Off Time	t_{OFF}		+25℃		20		ns
Break-Before-Make Time Delay	t_D	V_{IS} = 0.8V, R_L = 50Ω, C_L = 10pF, Test Circuit 3	+25℃		5		ns
Propagation Delay	t_{PD}	R_L = 50Ω, C_L = 10pF	+25℃		0.3		ns
Off Isolation	O_{ISO}	Signal = 0dBm, R_L = 50Ω, f = 250MHz, Test Circuit 4	+25℃		-30		dB
Channel-to-Channel Crosstalk	X_{TALK}	Signal = 0dBm, R_L = 50Ω, f = 250MHz, Test Circuit 5	+25℃		-33		dB
–3dB Bandwidth	BW	Signal = 0dBm, R_L = 50Ω, C_L = 5pF Test Circuit 6	+25℃		500		MHz
Channel-to-Channel Skew	t_{SKEW}	R_L = 50Ω, C_L = 10pF	+25℃		0.05		ns
Charge Injection Select Input to Common I/O	Q	V_G = GND, C_L = 1.0nF, R_G = 0Ω, Q = C_L x V_{OUT}, Test Circuit 7	+25℃		9.8		pC
HSD_+, HSD_-, D_+, D_- ON Capacitance	C_{ON}		+25℃		6.5		pF
POWER REQUIREMENTS							
Power Supply Range	V_+		-40℃ to +85℃	1.8		4.3	V
Power Supply Current	I_+	V_+ = 3.0V, V_S, $V_{\overline{OE}}$ = 0V or V_+	-40℃ to +85℃			1	μA

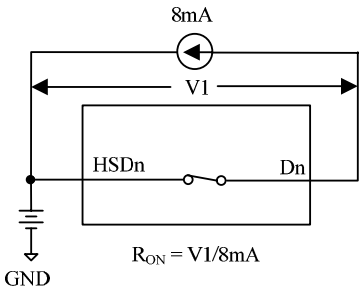
Specifications subject to changes without notice.

TYPICAL PERFORMANCE CHARACTERISTICS

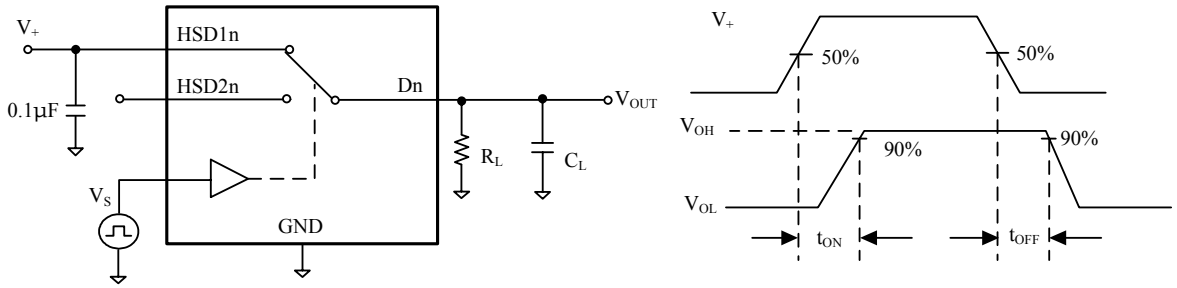




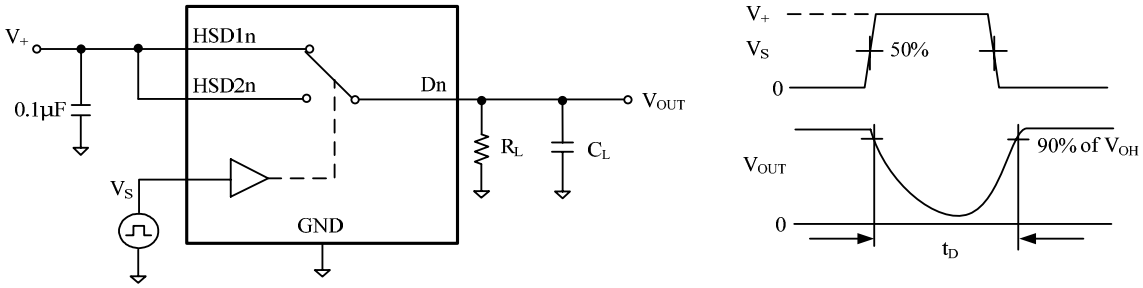
TEST CIRCUITS



Test Circuit 1. On Resistance

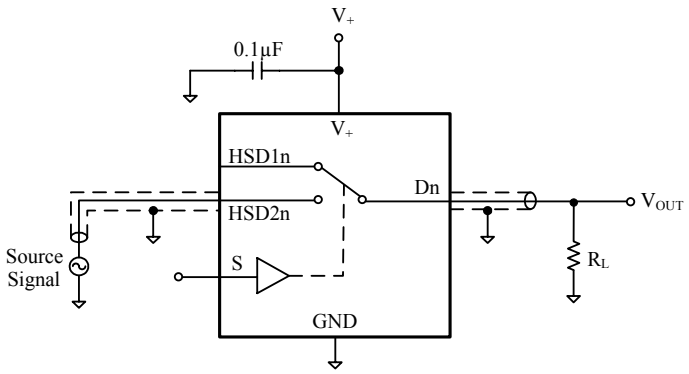


Test Circuit 2. Switching Times (t_{ON}, t_{OFF})

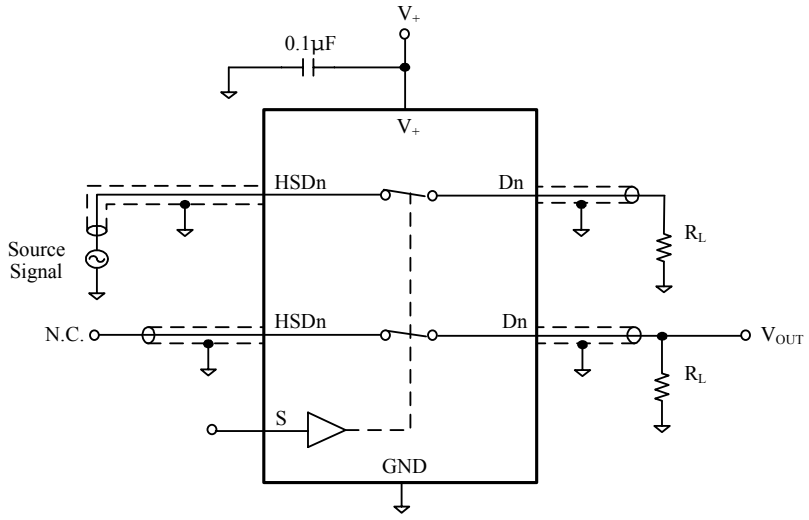


Test Circuit 3. Break-Before-Make Time (t_D)

TEST CIRCUITS (Cont.)



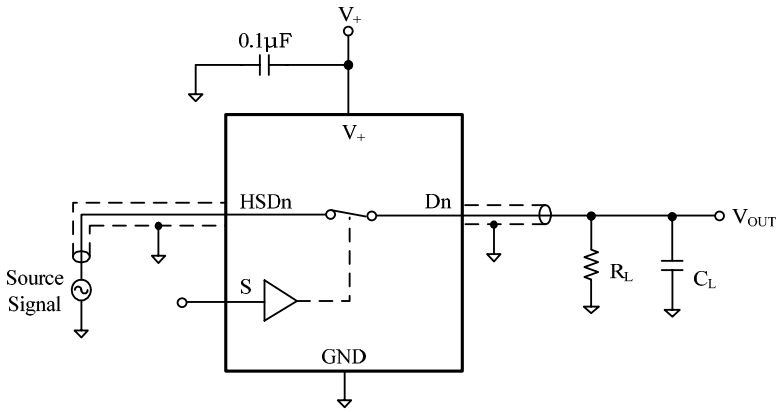
Test Circuit 4. Off Isolation



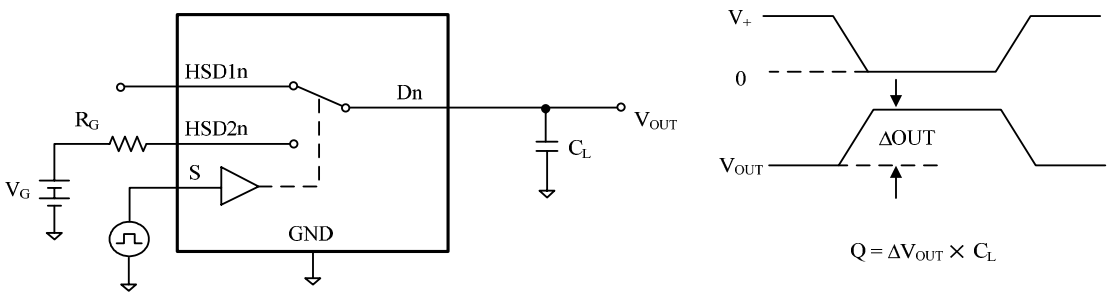
$$\text{Channel To Channel Crosstalk} = -20 \times \log \frac{V_{HSDn}}{V_{OUT}}$$

Test Circuit 5. Channel-to-Channel Crosstalk

TEST CIRCUITS (Cont.)



Test Circuit 6. -3dB Bandwidth



Test Circuit 7. Charge Injection (Q)

APPLICATION NOTES:

Meeting USB 2.0 V_{BUS} Short Requirements

In section 7.1.1 of the USB 2.0 specification, it notes that USB devices must be able to withstand a V_{BUS} short to D+ or D- when the USB devices is either powered off or powered on. The SGM7223 can be successfully configured to meet both these requirements.

Power-Off Protection

For a V_{BUS} short circuit, the switch is expected to withstand such a condition for at least 24 hours. The SGM7223 has specially designed circuitry which prevents unintended signal bleed through as well as guaranteed system reliability during a power-down, over-voltage condition. The protection has been added to the common pins (D+, D-).

Power-On Protection

The USB 2.0 specification also notes that the USB device should be capable of withstanding a V_{BUS} short during transmission of data. This modification works by limiting current flow back into the V+ rail during the over-voltage event so current remains within the safe operating range. In this application, the switch passes the full 5.25V input signal through to the selected output, while maintaining specified off isolation on the un-selected pins.

SGM7223 USB2.0 Signal Quality Compliance Tests

Figures 1 and 2 show the test results for USB eye diagram tests. A summary of the USB tests is provided in Table 1. The SGM7223 passes the high speed signal quality, eye diagram and jitter tests.

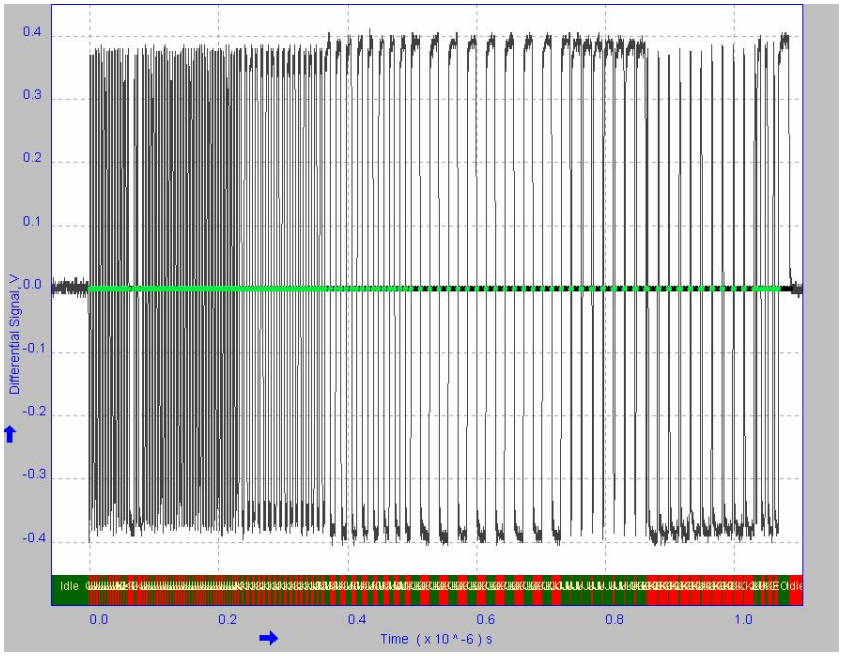


Figure 1. Waveform Plot

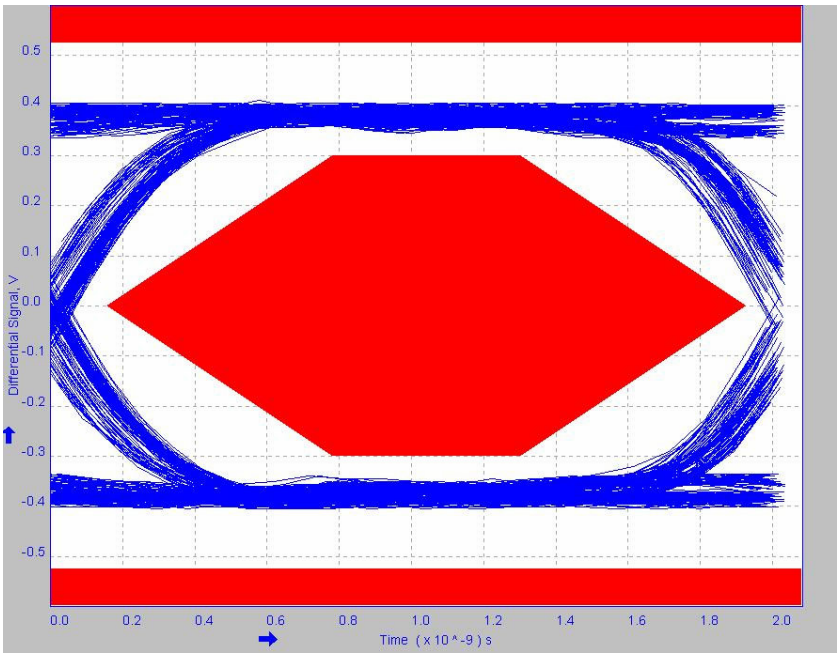


Figure 2. High Speed Signal Quality Eye Diagram Test (V+ = 3.3V)

SGM7223 USB2.0 Signal Quality Compliance Tests (Cont.)

Table 1. Summary of the USB 2.0 Signal Quality Tests Results

Measurement Name	MIN	MAX	Mean	pk-pk	Standard Deviation	RMS	Population	Status
Eye Diagram Test	-	-	-	-	-	-	-	Pass
Signal Rate	467.3807 Mbps	496.5449 Mbps	479.9494 Mbps	0.0000 bps	6.174360 Mbps	480.4821 Mbps	512	Pass
EOP Width	-	-	16.61442ns	-	-	-	1	Pass
EOP Width (Bits)	-	-	7.974082	-	-	-	1	Pass
Falling Edge Rate	1.100184 kV/μs	1.304518 kV/μs	1.187936 kV/μs	204.3340 V/μs	52.11665 V/μs	1.189068 kV/μs	107	Pass
Rising Edge Rate	1.058148 kV/μs	1.232657 kV/μs	1.137964 kV/μs	174.5099 V/μs	46.35985 V/μs	1.138899 kV/μs	108	Pass

Additional Information:

Consecutive Jitter range: -115.0ps to 71.20ps RMS Jitter 40.26ps

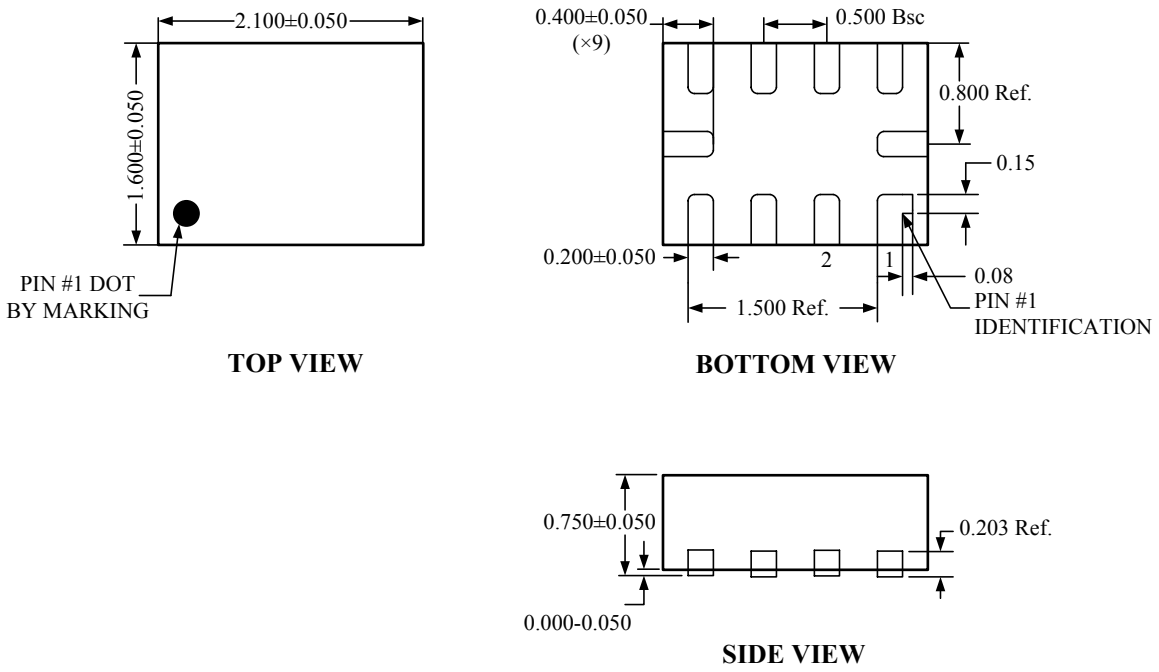
KJ Paired Jitter range: -34.68ps to 29.00ps RMS Jitter 11.09ps

JK Paired Jitter range: -30.42ps to 35.73ps RMS Jitter 12.11ps

- Rising Edge Rate: 1.137964kV/μs (Equivalent Rise Time = 562.41ps)
- Falling Edge Rate: 1.187936kV/μs (Equivalent Fall Time = 538.75ps)

PACKAGE OUTLINE DIMENSIONS

TQFN-10 (2.1mm×1.6mm)



Note: All linear dimensions are in millimeters.

REVISION HISTORY

Location **Page**

04/2008— Data Sheet REV. A

SGMICRO

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